EF

Notice of Allowability	Application No.	Applicant(s)	
	10/660,847	DHARNE ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 5/09/05*.

2. ☒ The allowed claim(s) is/are *2,4-12,14-16,18 and 20-26*.

3. ☒ The drawings filed on *16 November 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with David G. Dolezal on May 25, 2005.

The application has been amended as follows:

In line 1 of claim 18, the number "17" has been replaced with --16--.

In line 1 of claim 20, the number "19" has been replaced with --16--.

Allowable Subject Matter

2. Claims 2, 4-12, 14-16,18, and 20-26 are allowed.

3. The following is an examiner's statement of reasons for allowance: Claims 2, 4-6, 12 and 21-22 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the level shift circuitry further comprises: a first transistor (425) located in the first voltage domain and a second transistor (426) located in the second voltage domain in combination with the rest of the limitations of the base claims and any intervening claims. Claims 7-9 and 23 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the level shift circuitry comprises: a current path between the first signal terminal (ST1) and the second signal terminal (ST2), the current path including a first transistor (325) and a

second transistor (327), the first transistor (325) being disposed within the first voltage domain and having a first current terminal coupled to the first signal terminal (ST1), a control terminal coupled to a first voltage domain voltage supply (V_{DD1}), and a second current terminal, and the second transistor (327) being disposed within the second voltage domain and having a first current terminal coupled to the second signal terminal (ST2), a control terminal coupled to a second voltage domain voltage supply (V_{DD2}), and a second current terminal coupled to the second current terminal of the first transistor (325) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 10 and 24 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the level shift circuitry further comprises: a first transistor (323) located in the first voltage domain and having a first current terminal coupled to a first voltage domain voltage supply and a second current terminal coupled to the first signal terminal; a second transistor (321) located in the first voltage domain and having a first current terminal coupled the first voltage domain voltage supply, a second current terminal coupled to the control terminal of the first transistor, and a control terminal coupled to the first signal terminal; a third transistor (311) located in the second voltage domain and having a first current terminal coupled to a second voltage domain voltage supply and a second current terminal coupled to the second signal terminal; a fourth transistor (313) located in the second voltage domain and having a first current terminal coupled the second voltage domain voltage supply, a second current terminal coupled to the control terminal of the third transistor, and a control terminal coupled to the second signal terminal in combination

with the rest of the limitations of the base claims and any intervening claims. Claims 11 and 25 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the circuit further comprises a first circuit (331) including circuitry to enable the first circuit to receive the shifted signal from the first signal terminal and circuitry to enable the first circuit to provide the first signal and a second circuit (341) including circuitry to enable the second circuit to receive the shifted signal from the second signal terminal and circuitry to enable the second circuit to provide the second signal in combination with the rest of the limitations of the base claims and any intervening claims. Claims 15 and 14 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the circuit further comprises enabling circuitry (331) of a first circuit in combination with the rest of the limitations of the base claims and any intervening claims. Claims 16, 18, 20, and 26 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 5 wherein the circuit includes a bias circuit (529) coupled to the gate of a first transistor (525) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

May 25, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800